

REMARKS

We hereby request that the suspension of this Application be lifted.

Claim 18 has been added to better scope the invention. Claim 5 has been amended to correct a typographical error, and claims 2, 5 and 7 have been amended to employ more idiomatic English. No new matter has been entered.

Turning to the art rejections, the rejection of claims 1 and 2 as anticipated by Uchida et al. or by Hidaka et al. is in error. In formulating his rejections, the Examiner is applying hindsight reasoning based on unfounded assumptions. Specifically, neither Uchida et al. nor Hidaka et al. teach setting the gate length longer than a half pitch, i.e., the minimum processing dimension, which is required by claim 1. Instead, Uchida et al. teaches setting the gate length longer than 2 μ m (Column 12, lines 5-7) and Hidaka et al. teaches a gate length longer than 0.20 microns (Column 2, lines 26-29 and column 4, lines 29-30). That is, both references teach setting the gate length longer than some absolute length, and neither teaches the length of the gate electrode in relation to the half pitch.

To support his rejection, the Examiner claims a similar sounding term in each of the references is equal to the Applicants' minimum processing dimension. Applicants agree with the Examiner that the Applicants' Admitted Prior Art (AAPA) defines the half pitch equal to the minimum processing dimension F. However, Applicants cannot find any support in any of the cited references for the Examiner's conjecture that the "minimum design dimension" of Hidaka et al. and the "minimum processable size" of Uchida et al. are synonyms for "minimum processing dimension." Thus, claims 1 and 2 are not anticipated or for that matter rendered obvious by Uchida et al. or Hidaka et al.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

175 CANAL STREET
MANCHESTER, NH 03101
TEL. 603.668.1400
FAX. 603.668.8567

The Examiner's rejection of claims 3-4 and 5-6 under 35 USC §103(a) as being obvious over Applicants' AAPA in view of Bronner et al. (US Patent No. 6,767,789) also is in error. Claims 3-4 and 5-6 indirectly depend on independent claim 1, and are patentable for the reasons above as well as for their own limitations. Furthermore, the Examiner claims Bronner et al. discloses setting a gate length longer than the half pitch. However, Bronner actually teaches "the gate length must be designed longer than the minimum dimension" but never defines the minimum dimension (column 2, lines 53-54). As in the other rejections, the Examiner assumes "minimum dimension" of Bronner is equal to Applicants' "minimum processing dimension" without any support in any of the cited references.

Furthermore, Bronner et al. teaches away from using a gate longer than a minimum dimension. Bronner et al. states a longer gate length "makes it almost impossible to effectively reduce the size of the DRAM cell." (Column 2, lines 50-58) and therefore Bronner et al. teaches away from Applicants' invention. Thus, claims 3-4 and 5-6 are patentable over the combination of AAPA and Bronner et al.

Turning to the rejection of claims 7 and 8 as being obvious from Hidaka et al., claims 7 and 8 are both directly dependent on claim 1. The deficiencies of Hidaka et al. vis-à-vis claim 1 are discussed above. Thus, claims 7 and 8 are patentable over Hidaka et al. for the same reasons above adduced relative to claim 1 as well as for their own additional limitations.

Finally, none of the cited art teaches the shortest distance between the first diffusion layer and the second diffusion layer is greater than a half pitch, as required by new independent claim 18. Thus, claim 18 is not anticipated or for that matter rendered obvious by any combination of AAPA, Bronner, Uchida et al. and Hidaka et al.

HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
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FAX. 520.882.7643

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New claim 18 is allowable over the applied art for the same reasons above adduced for claims 1-8, as well as for their own additional limitations.

Having dealt with all the objections raised by the Examiner, the Application is believed to be in order for allowance. Early and favorable action is respectfully requested.

In the event there are any fee deficiencies or additional fees are payable, please charge them (or credit any overpayment) to our Deposit Account Number 08-1391.

Respectfully submitted,



Norman P. Soloway
Attorney for Applicants
Reg. No. 24,315

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I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: MAIL STOP AMENDMENT, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on March 16, 2006, at Tucson, Arizona.

By 

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HAYES SOLOWAY P.C.
3450 E. SUNRISE DRIVE
SUITE 140
TUCSON, AZ 85718
TEL. 520.882.7623
FAX. 520.882.7643

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